**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| **Applicant:** | **Vijay K. Reddy, et al.** | **Art Unit:** | **2858** |
| **Serial No.:** | **10/814,453** | **Examiner:** | **Jeff W. Natalini** |
| **Filed:** | **03/31/04** | **Docket:** | **TI-37048** |
| **For:** | **VOLTAGE WAVEFORM GENERATION CIRCUIT** | | |

**AMENDED APPEAL BRIEF SUMMARY OF CLAIMED SUBJECT MATTER**

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Amended Summary of Claimed Subject Matter in connection with the above-identified application in response to the Notification of Non-Compliant Appeal Brief mailed **August 24, 2007**.

## SUMMARY OF CLAIMED SUBJECT MATTER

Specification page 6, line 7 to page 10, line 23, provides a concise explanation of the invention defined in claim 1.

The step of processing a request for a voltage overshoot or undershoot in claim 1 is accomplished by element 406 in Figure 4.

The step of applying the plurality of inputs to a waveform generation circuit in claim 1 is accomplished by elements 408 and 410 in Figure 4.

The step of generating a voltage waveform in claim 1 is accomplished by element 412 in Figure 4.

Referring now to Figure 3, an exemplary test methodology 300 is shown in accordance with embodiments of the invention. As can be appreciated, the ability to inject overshoots and undershoots into a circuit under test in accordance with embodiments of the invention may lead to the development of more accurate circuit reliability models. Such models may be used for channel-hot-carrier (CHC) degradation, negative bias temperature instability (NBTI), gate oxide reliability, and electro-migration. The test methodology 300 for generating such models may inject voltage overshoots and/or undershoots into the circuit under test for a period of time commonly referred to as the "stress interval." Before the stress interval, a pre-stress characterization measurement may be taken of the device under test (block 302). The measurement may determine the

frequency of oscillation and the quiescent state of current (IDDQ) through the power supply line ($V_{DD}$) of the device under test. During the stress interval, additional characterization measurements of the frequency of oscillation and the quiescent state of current through the power supply line may be obtained (block 306). The stress interval may end after a predetermined time period or a measurable condition, such as circuit failure, occurs (block 308). After the stress interval, a post-stress measurement may be obtained (block 310). Comparing the pre-stress characterization measurement, the characterization measurements obtained during the stress interval, and the post-test characterization measurement may reveal if and when the device under test begins to behave abnormally. The comparison may be accomplished, for example, by plotting the characterization measurements to produce graphs that reveal the behavior of the circuit under test before, after, and during the stress interval.

Referring now to Figure 4, a block diagram of an exemplary waveform generation system 400 is shown in accordance with embodiments of the invention. As shown, a user 402 may select waveform parameters 404 describing a voltage waveform desired to be generated. The waveform parameters 404 preferably comprise the following five parameters: the type of waveform (e.g., an overshoot or undershoot), the magnitude of the waveform, the duration of the waveform, the frequency of the waveform, and the duty cycle of the waveform. Although typically all five parameters are selected by the user 402, certain combinations of parameters may also be selected by processing software 406. For example, an overshoot may be selected with defined magnitude, duration, and frequency parameters. The processing software 406 may determine an appropriate duty cycle for the overshoot or select an arbitrary duty cycle. The processing software 406

processes the waveform parameters 404 into a request 408 that is sent on a communications bus 410, such as an inter-IC ($I^2C$) bus, to a waveform generation circuit 412. The generation circuit 412 utilizes the request 408 to generate an output waveform 414. The output waveform 412 may be applied to any desired electrical device under test 416 (DUT), such as a transistor or capacitor.

Figure 5 depicts a procedure 500 for generating voltage waveforms in accordance with embodiments of the invention. The procedure 500 may start by connecting the device 414 to the waveform generation circuit (block 502). After the connection has been established, waveform parameters 404 may be selected (block 504). As previously discussed, the waveform parameters 404 may comprise the type of waveform (e.g., an overshoot or undershoot), the magnitude of the waveform, the duration of the waveform, the frequency of the waveform, and the duty cycle of the waveform. After selection of the waveform parameters 404, the processing software 406 may process the waveform parameters 404 into a request 408 (block 505). The request 408 may be sent on the bus 410 to the waveform generation circuit 412 (block 506). The request 408 may be applied to the waveform generation circuit 412 to generate a waveform corresponding to the parameters 404 (block 508).

Referring now to Figure 6, a block diagram of an exemplary waveform generation circuit 600 that is capable of producing voltage overshoots is shown. As shown, the waveform generation circuit 600 comprises a current regulator 602, a controlled oscillator 604, a clock 606, a discharge device 608, a comparator 610, a programmable delay circuit 612, and a device under test 614.

The current regulator 602 preferably comprises a voltage and temperature invariant charge pump that outputs current proportional to the frequency of the controlled oscillator 604. The clock 606 and the controlled oscillator 604 preferably operate in the gigahertz ($10^9$ hertz) frequency range in order to produce voltage waveforms that overshoot the settled value for a duration on the order of picoseconds ($10^{-12}$ seconds). The clock 606 may comprise a phase locked loop (PLL) circuit, or any other type of controllable oscillator. The comparator 610 preferably possesses a fast switching to minimize the timing propagation into the programmable delay circuit 612. The programmable delay circuit 612 may comprise a chain of inverters, each inverter preferably representing approximately 20 picoseconds of delay. The frequency of the oscillator 604 may be controlled by an input 616, the period of delay caused by the programmable delay circuit 612 may be controlled by an input 618, and the frequency of the clock 606 may be controlled by an input 610.

Depending upon the voltage applied to the input 616, the oscillator 604 may produce a signal with a known frequency of oscillation. When a rising edge of the clock 606 enables the current regulator 602, the signal produced by the controlled oscillator 604 may cause the current regulator 602 to charge the $V^+$ node of the comparator, thereby increasing the voltage of the device under test ($V_{DUT}$). When the $V^+$ node of the comparator 610 becomes greater than the reference voltage $V_{REF}$ applied to the $V^-$ node, a delay is instantiated by the programmable delay circuit 612. During the delay, the current regulator 602 may continue to increase the voltage of the device under test ($V_{DUT}$) to a value of $V_{DDSTRESS}$. After the delay, a discharge mechanism is instantiated by the discharge device 608. During the discharge, the voltage of the device under test ($V_{DUT}$) is

reduced to a nominal $V_{DD}$ value. When a falling edge of the clock 606 disables the current regulator 602, the voltage of the device under test ($V_{DUT}$) is discharged to approximately zero volts. The process of charging and discharging the voltage of the device under test ($V_{DUT}$) may repeat ever cycle of the clock 606.

The input 616, the input 618, the input 620, the reference voltage $V_{REF}$, and the stress voltage $V_{DDSTRESS}$ may be used to produce a desired overshoot voltage waveform at the $V_{DUT}$ node that is in accordance with the waveform parameters 404 selected by a user. The current regulator 602 controls the magnitude of the overshoot via the $V_{DDSTRESS}$ signal, the programmable delay circuit 612 controls the duration of the overshoot via the input 618, the clock 606 controls the frequency of waveform and the duty cycle of the waveform via the input 620.

Figure 8 illustrates an exemplary circuit-level implementation of the waveform generation circuit 600. The circuit is constructed using the components discussed in the foregoing discussion. More specifically, a current regulator 802 is coupled to a voltage comparator 804. The comparator 804 generates a rising edge once node $V_+$ is greater than $V_{REF}$. A set-reset (S/R) flip-flop 806 triggers the discharging transistor attached to node $V_+$ after an insertion delay introduced by a programmable delay circuit 808. Thus, the actual value of the overshoot voltage may be set by the value of $V_{REF}$ and the duration of the overshoot may be set by the programmable delay circuit 808.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

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